2. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the axis is not generally perpendicular with an orthogonal edge of the substrate.

3. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the substrate comprises a processor.

4. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the substrate comprises a memory device.

5. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the substrate comprises an integrated circuit device.

6. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein each of the plurality of capacitive memory elements is generally oblong in shape.

7. (Original) The plurality of capacitive memory elements set forth in claim 6, wherein each of the plurality of capacitive memory elements is generally ellipsoidal.

8. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein each of the plurality of capacitive memory elements is slanted with respect to the edge of the substrate.

9. (Original) A plurality of capacitive memory elements arranged in a first row and a second row so that an axis through any of the plurality of capacitive memory elements located in the first row does not form an axis of any capacitive memory element in the second row.

10. (Original) The plurality of capacitive memory elements set forth in claim 9 wherein the plurality of capacitive memory elements is disposed on a substrate.

11. (Original) The plurality of capacitive memory elements set forth in claim 9 wherein the axis is not generally parallel with an edge of the substrate.

12. (Original) The plurality of capacitive memory elements set forth in claim 11 wherein the axis is not generally perpendicular with an orthogonal of the substrate.

13. (Original) The plurality of capacitive memory elements set forth in claim 9 wherein the substrate comprises a processor.

14. (Original) The plurality of capacitive memory elements set forth in claim 9 wherein the substrate comprises a memory device.

15. (Original) The plurality of capacitive memory elements set forth in claim 9 wherein the substrate comprises an integrated circuit device.

16. (Original) The plurality of capacitive memory elements set forth in claim 9 wherein the axis is slanted with respect to the edge of the substrate.

17. (Original) The plurality of capacitive memory elements set forth in claim 9 wherein each of the plurality of capacitive memory elements is generally oblong in shape.

18. (Original) The plurality of capacitive memory elements set forth in claim 17, wherein each of the plurality of capacitive memory elements is generally ellipsoidal.

19. (Original) The plurality of capacitive memory elements set forth in claim 9 wherein the axis is a longitudinal axis through one of the capacitive memory elements.

20. (Original) An integrated circuit device, comprising:

a substrate;

a memory array that includes a plurality of memory cells disposed on the substrate, the memory array comprising a plurality of capacitive memory elements, each of the capacitive memory elements being associated with one of the plurality of memory cells, the plurality of capacitive memory elements being disposed on the substrate so that an axis that runs longitudinally through one of the plurality of capacitive memory elements is not generally parallel with an edge of the substrate.

21. (Original) The integrated circuit device set forth in claim 20 wherein the axis is not generally perpendicular with an orthogonal edge of the substrate.

22. (Original) The integrated circuit device set forth in claim 20 wherein the substrate comprises a processor.

23. (Original) The integrated circuit device set forth in claim 20 wherein the substrate comprises a memory device.

24. (Original) The integrated circuit device set forth in claim 20 wherein each of the plurality of capacitive memory elements is generally oblong in shape.

25. (Original) The plurality of capacitive memory elements set forth in claim 24, wherein each of the plurality of capacitive memory elements is generally ellipsoidal.

26. (Original) The integrated circuit device set forth in claim 20 wherein each of the plurality of capacitive memory elements is slanted with respect to the edge of the substrate.

27. (Original) An integrated circuit device, comprising:

a substrate;

a memory array that includes a plurality of memory cells disposed on the substrate, the memory array comprising a plurality of capacitive memory elements, each of the capacitive memory cells being associated with one of the plurality of memory cells, the plurality of capacitive memory elements being arranged in a first row and a second row so that an axis through one of the plurality of capacitive memory elements located in the first row does not form an axis of any capacitive memory element in the second row.

28. (Original) The integrated circuit device set forth in claim 24 wherein the plurality of capacitive memory elements is disposed on a substrate.

29. (Original) The integrated circuit device set forth in claim 24 wherein the axis is not generally parallel with an edge of the substrate.

30. (Original) The integrated circuit device set forth in claim 26 wherein the axis is not generally perpendicular with an orthogonal edge of the substrate.

31. (Original) The integrated circuit device set forth in claim 24 wherein the substrate comprises a processor.

32. (Original) The integrated circuit device set forth in claim 24 wherein the substrate comprises a memory device.

33. (Original) The integrated circuit device set forth in claim 24 wherein each of the plurality of capacitive memory elements is slanted with respect to the edge of the substrate.

34. (Original) The integrated circuit device set forth in claim 24 wherein each of the plurality of capacitive memory elements is generally oblong in shape.

35. (Original) The integrated circuit device set forth in claim 31, wherein each of the plurality of capacitive memory elements is generally ellipsoidal.

36. (Original) The integrated circuit device set forth in claim 24 wherein the axis is a longitudinal axis.

37-57. (Cancelled)